CS6133 Software Specification and Verification

Spring 2014

Course Instructor:

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Course Meetings: TR 7:30 pm – 8:45 pm in classroom UTSA-1604 FLN 1.02.08

Office Hours: TR 4:00 pm – 5:30 pm

Course Web Page: http://www.cs.utsa.edu/~niu/teaching/cs6133

Required Textbook


Course Outline

This course introduces the theory and practice of formal methods for the specification and verification of computer-based systems. It emphasizes various techniques for modeling system behavior and detecting in the model subtle errors that would be difficult and time-consuming to find in an implementation. Some automated analysis tools that have been applied successfully in checking the correctness of specifications are reviewed in this course.

Course Goals

• To learn how to specify software systems using formal modeling notations
• To study a variety of verification techniques
• To gain hands-on experience with verification tools

Course Topics

• Specification notations and their semantics
• Temporal logics, BDDs, SAT solving, and model checking
• Automated analysis techniques tools
Grading Scheme

- Quizzes: 10%
- Midterm: 20%
- Individual Assignment: 15%
- Presentation: 15%
- Group Project: 30%
- Participation: 10%

Examination Schedule

- TBD

No makeup exams will be permitted.

This Syllabus is provided for informational purposes regarding the anticipated course content and schedule of this course. It is based upon the most recent information available on the date of its issuance and is as accurate and complete as possible. I reserve the right to make any changes I deem necessary and/or appropriate. I will make my best efforts to communicate any changes in the syllabus in a timely manner. Students are responsible for being aware of these changes.

The common syllabus information and Roadrunner Creed can be found at http://utsa.edu/syllabus.