

CS6133 Software Specification and Verification

Fall 2011

Course Instructor:

Name: Jianwei Niu

Office: SB 4.01.36

Email: niu@cs.utsa.edu

Course Meetings: T/T 7:00 - 8:15 pm, **SB 3.02.10A**

Office Hours: Tuesday 5:00 - 7:00 pm

Course Web Page: <http://www.cs.utsa.edu/~niu/teaching/cs6133>

Required Textbook:

Michael Huth and Mark Ryan, "Logic in Computer Science", Cambridge University Press, 2004.

Course Description:

This course introduces the theory and practice of formal methods for the specification and verification of computer-based systems. It emphasizes various techniques for modeling system behavior and detecting in the model subtle errors that would be difficult and time-consuming to find in an implementation. Some automated analysis tools that have been applied successfully in checking the correctness of specifications are reviewed in this course.

Course Goals:

- To learn how to specify software systems using formal modeling notations
- To study a variety of verification techniques
- To gain hands-on experience with verification tools

Course Topics:

- Specification notations and their semantics
- Temporal logic, BDDs, SAT solver, and model checking
- Automated analysis tools

Grading Scheme:

- Quizzes: 15%
- Individual Assignment: 10%
- Presentation: 15%
- Participation: 10%
- Project: 40%