POWER MANAGEMENT AND DYNAMIC VOLTAGE SCALING: MYTHS AND FACTS

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INTRODUCTION

Dynamic Voltage Scaling

- used for power management
- often based on naïve system power models

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- real measurements
- 14 macro-benchmarks
- run on real hardware (not simulators)

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Analysis

- real measurements
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Results

- real measurements differ dramatically from naïve models
- optimum dependent on workload

NAÏVE POWER MODEL

Basis *dynamic* switching power P of CMOS circuits:

$$P \propto f V^2$$

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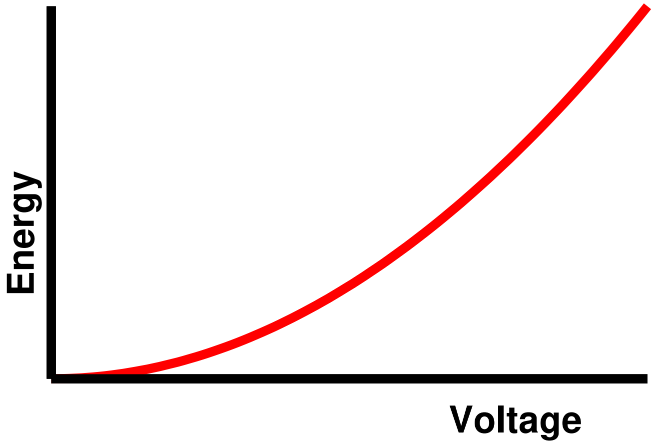
Assumption: # cycles for computation is independent of f_{core}

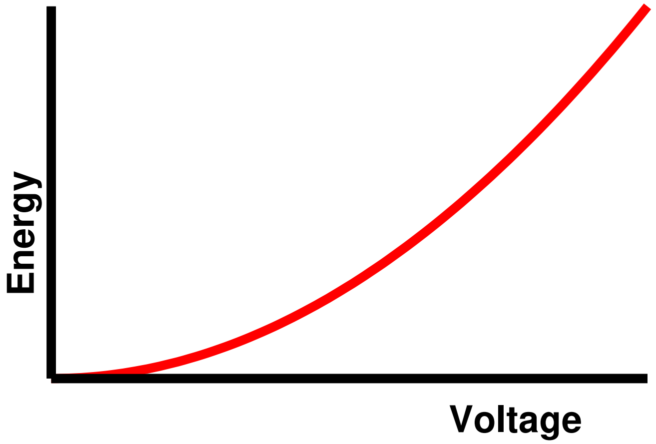
$$E \propto V^2$$



NAÏVE POWER MODEL

Limitations of the naïve power model:

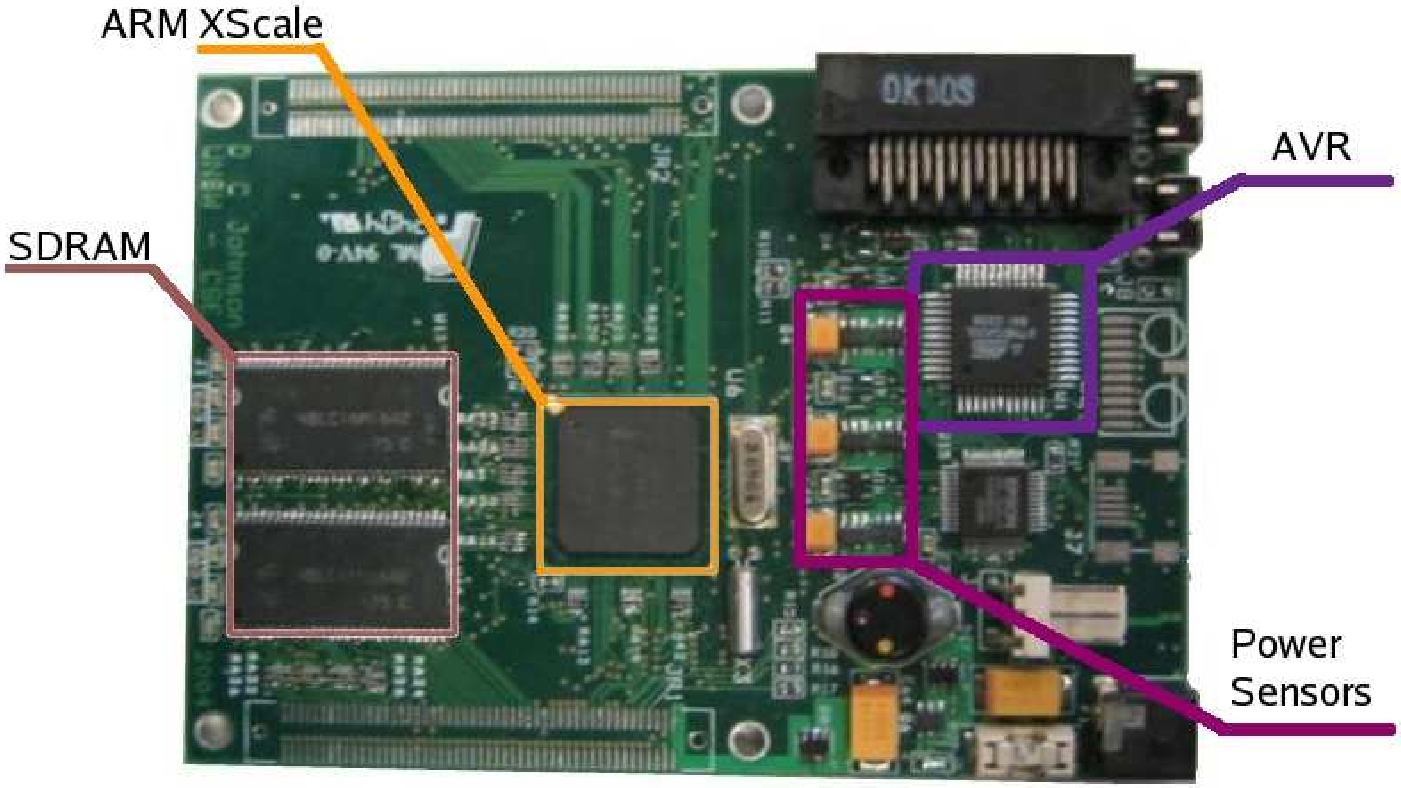
- ➜ ignores static power
- ➜ ignores other components: memory and busses
  - they affect execution time, consume energy
  - their energy consumption scales differently than CPU



HARDWARE PLATFORM

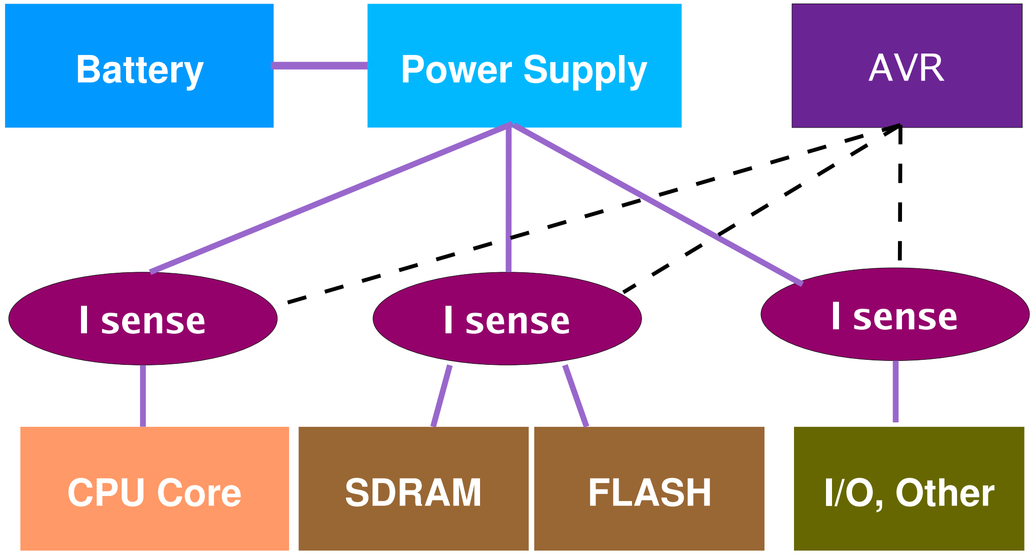
PLEB 2:

- ➜ Single board computer based on Intel XScale (PXA255)
- ➜ Representative of a typical embedded system



HARDWARE PLATFORM

- ➜ Three power supplies: CPU, Memory and IO
- ➜ Each power supply's current is measured
- ➜ On-board micro-controller (AVR) for monitoring
- ➜ Samples taken periodically according to AVR clock
- ➜ $f_{\max}$ samples is 15 KHz, subdivided into three channels



BENCHMARKS AND V/F CONFIGURATIONS

14 Macro-benchmarks:

- ➜ most from MiBench, selected according to resource limitations
- ➜ automotive, industrial control, network, office, signal processing
- ➜ plus 4 more: gzip, MP3, image analysis, speech compression

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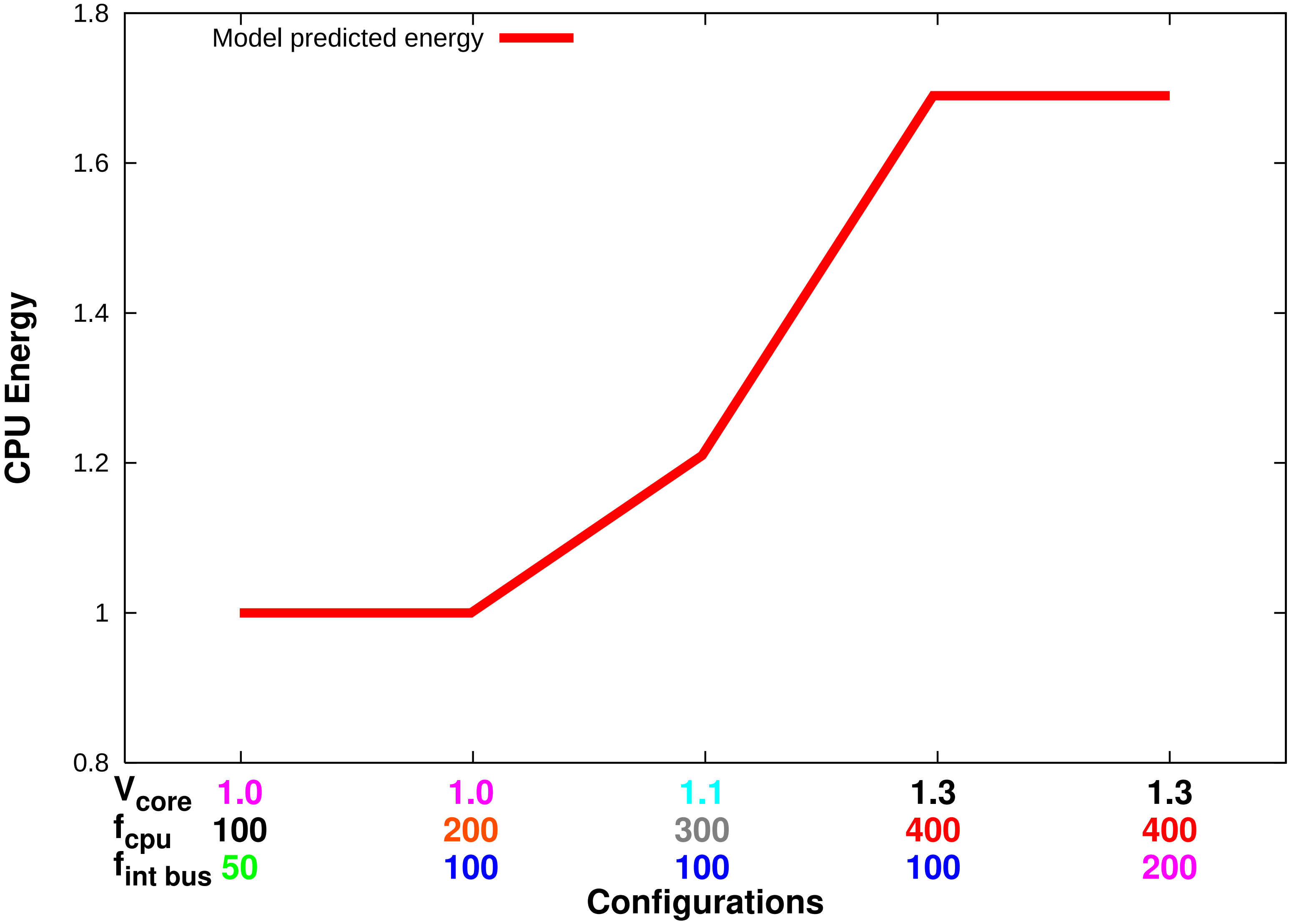
Valid voltage/frequency configurations for ARM XScale:

V_{core} (V)	f_{cpu} (MHz)	$f_{internalbus}$ (MHz)	f_{mem} (MHz)
1.0	100	50	100
1.0	200	100	100
1.1	300	100	100
1.3	400	100	100
1.3	400	200	100

1. NORMALIZED CPU ENERGY MODEL



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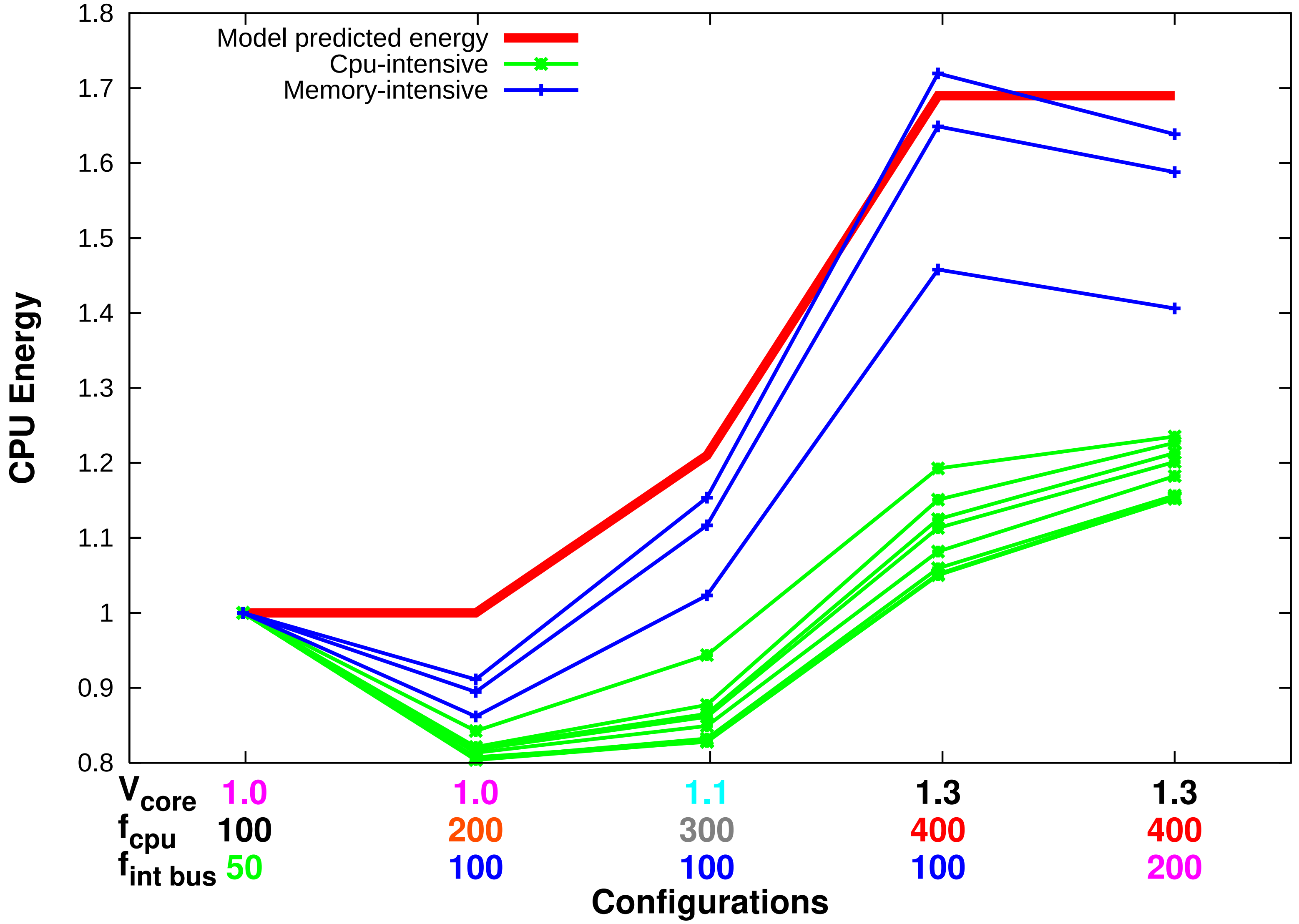
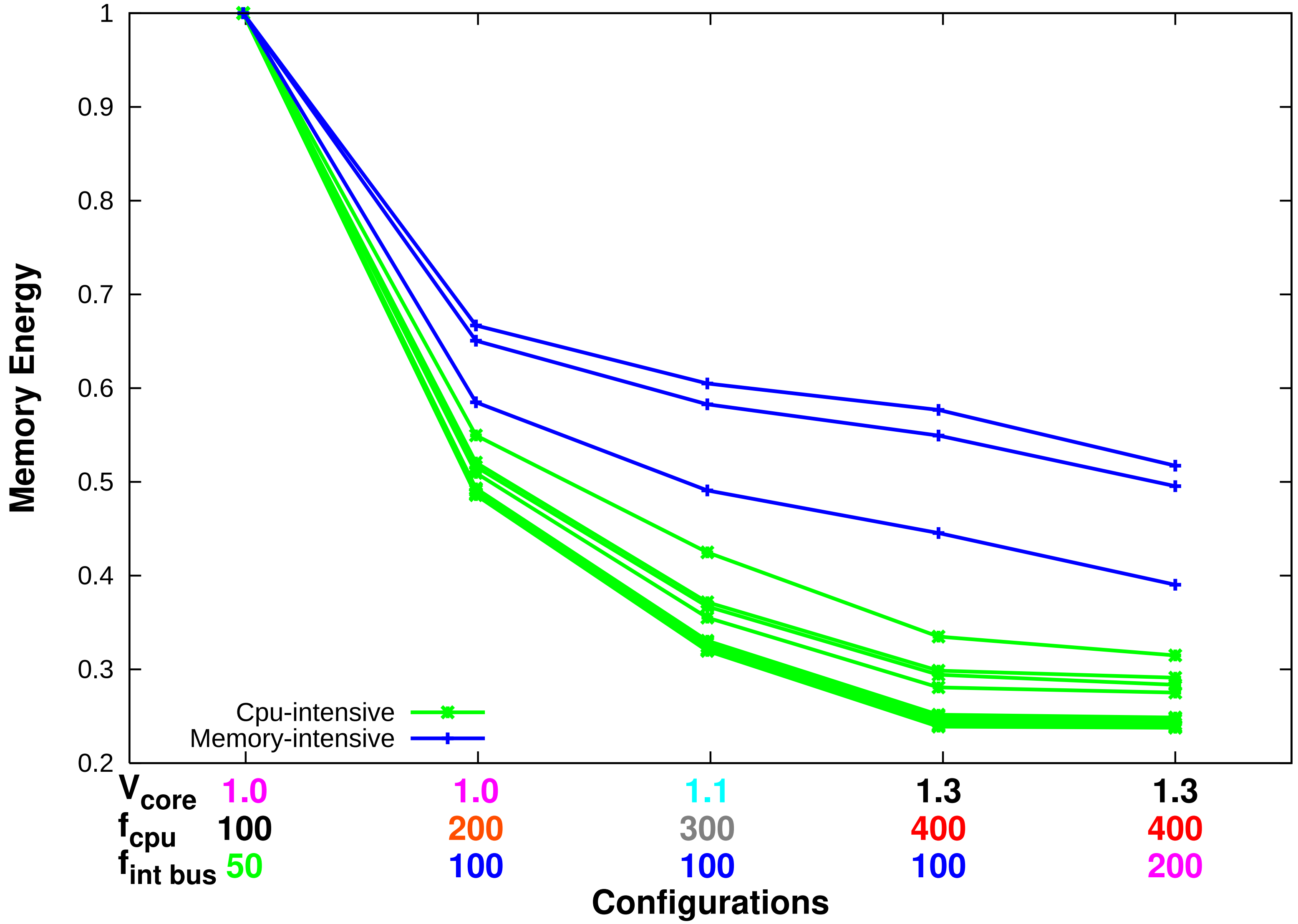
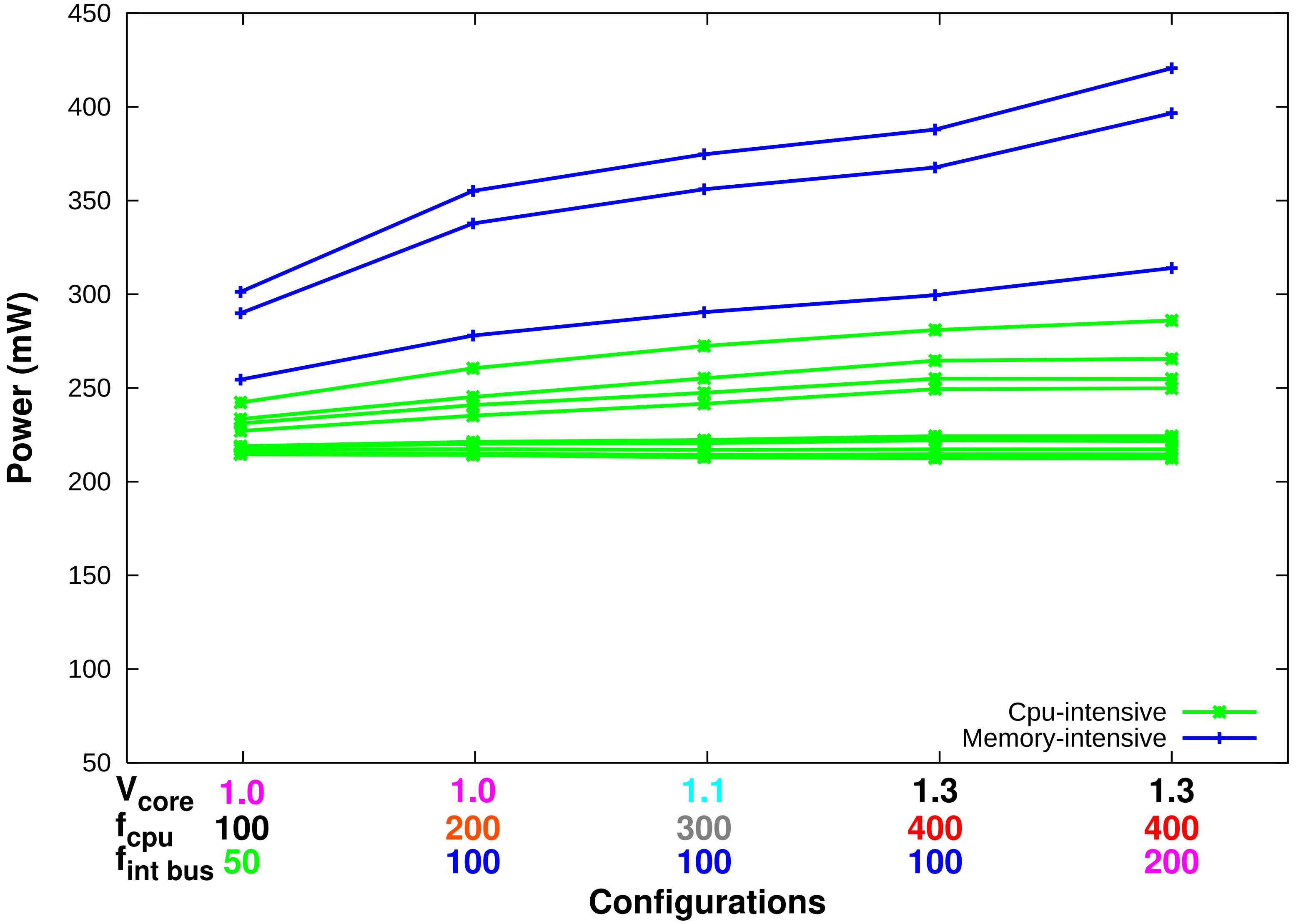


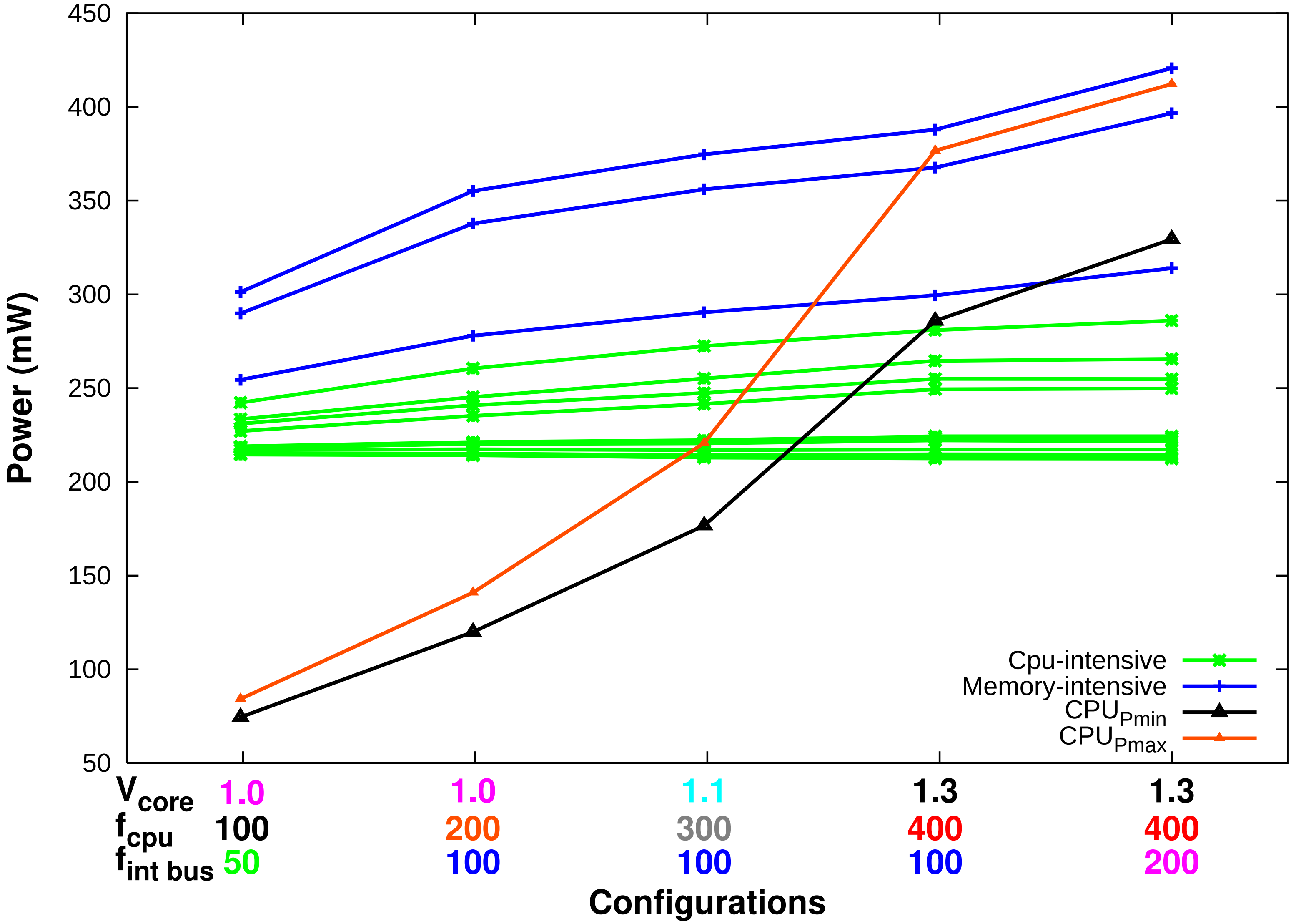
1.B NORMALIZED MEMORY ENERGY



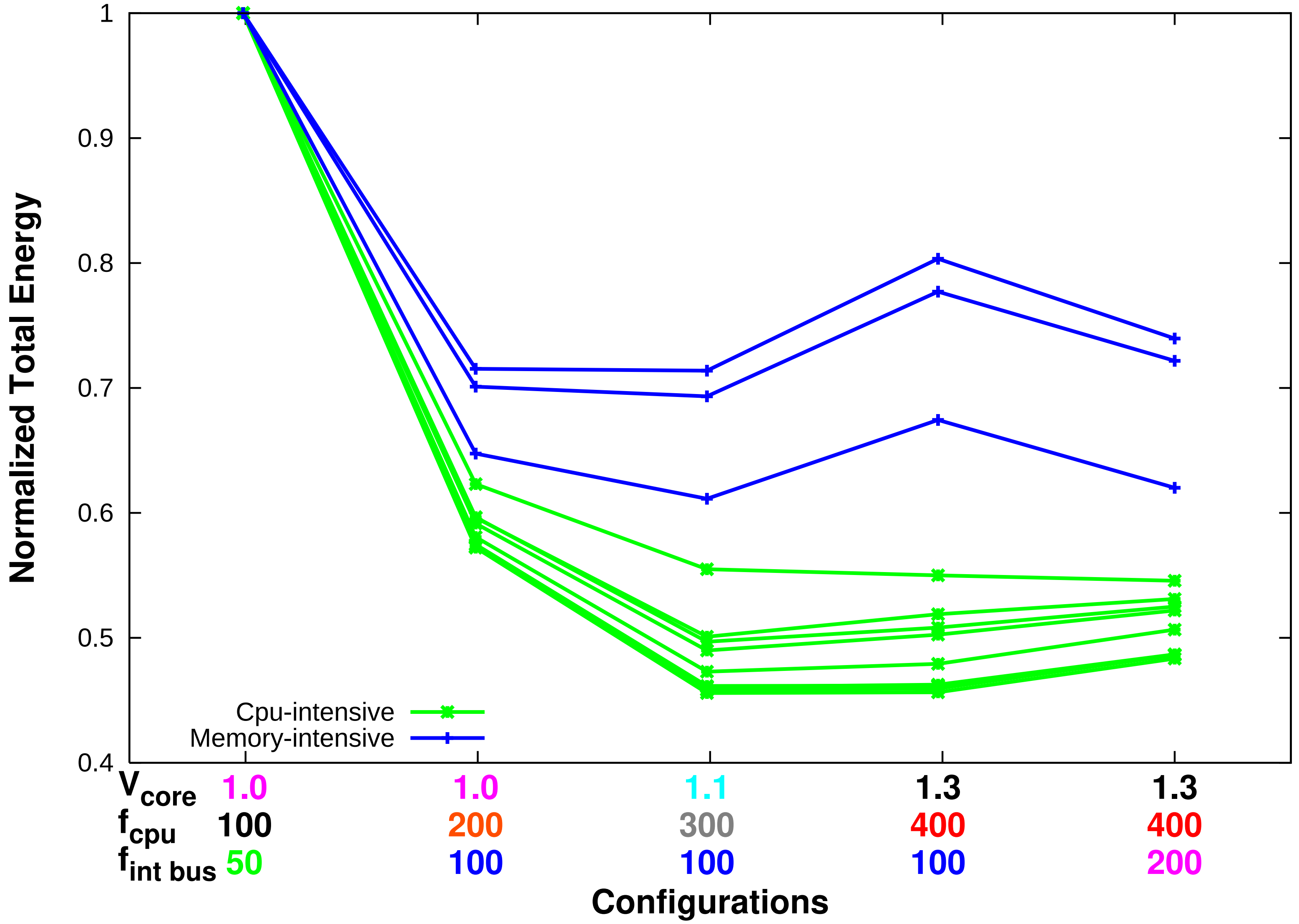
2. MEMORY POWER



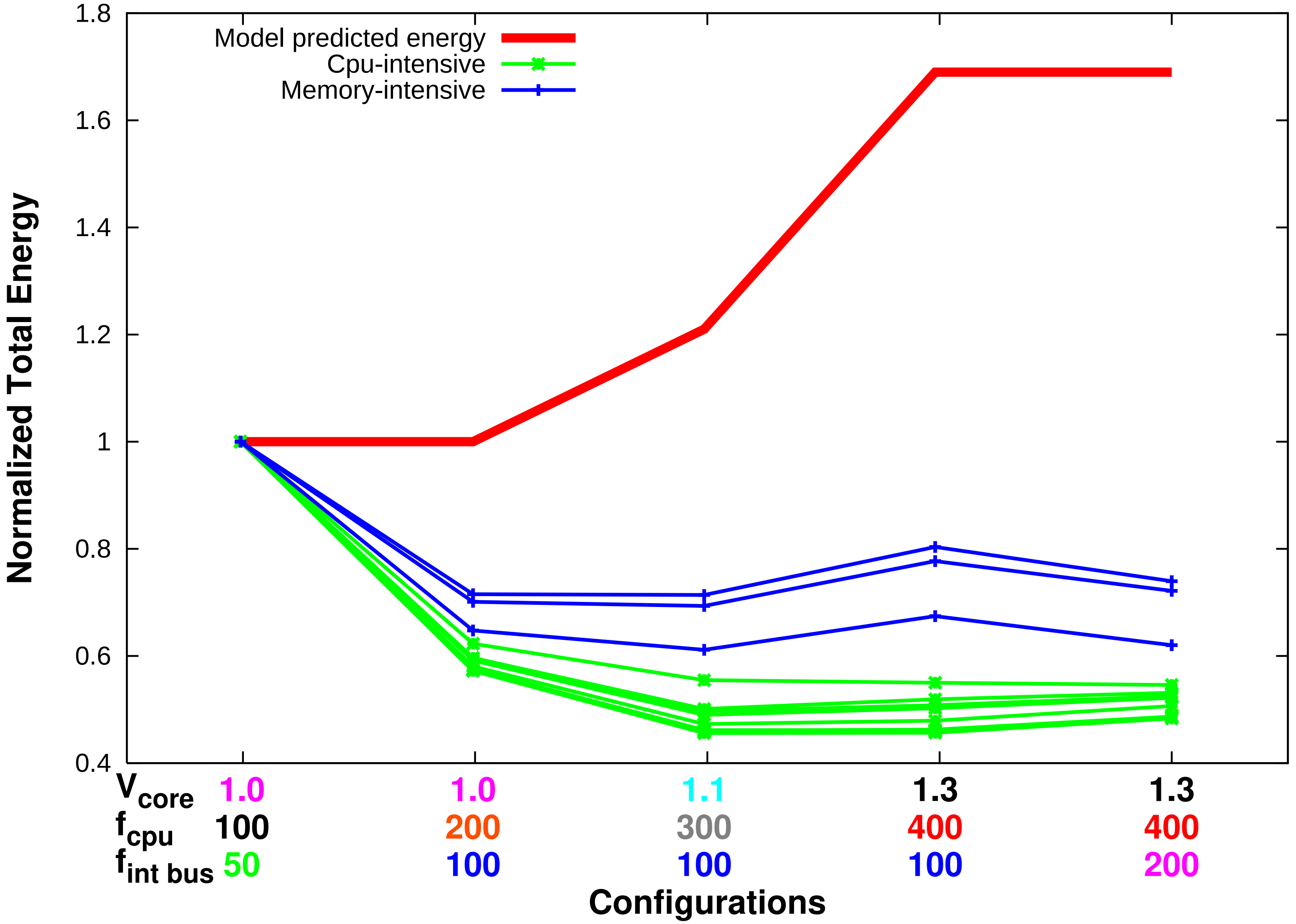
2. MEMORY POWER VS CPU POWER



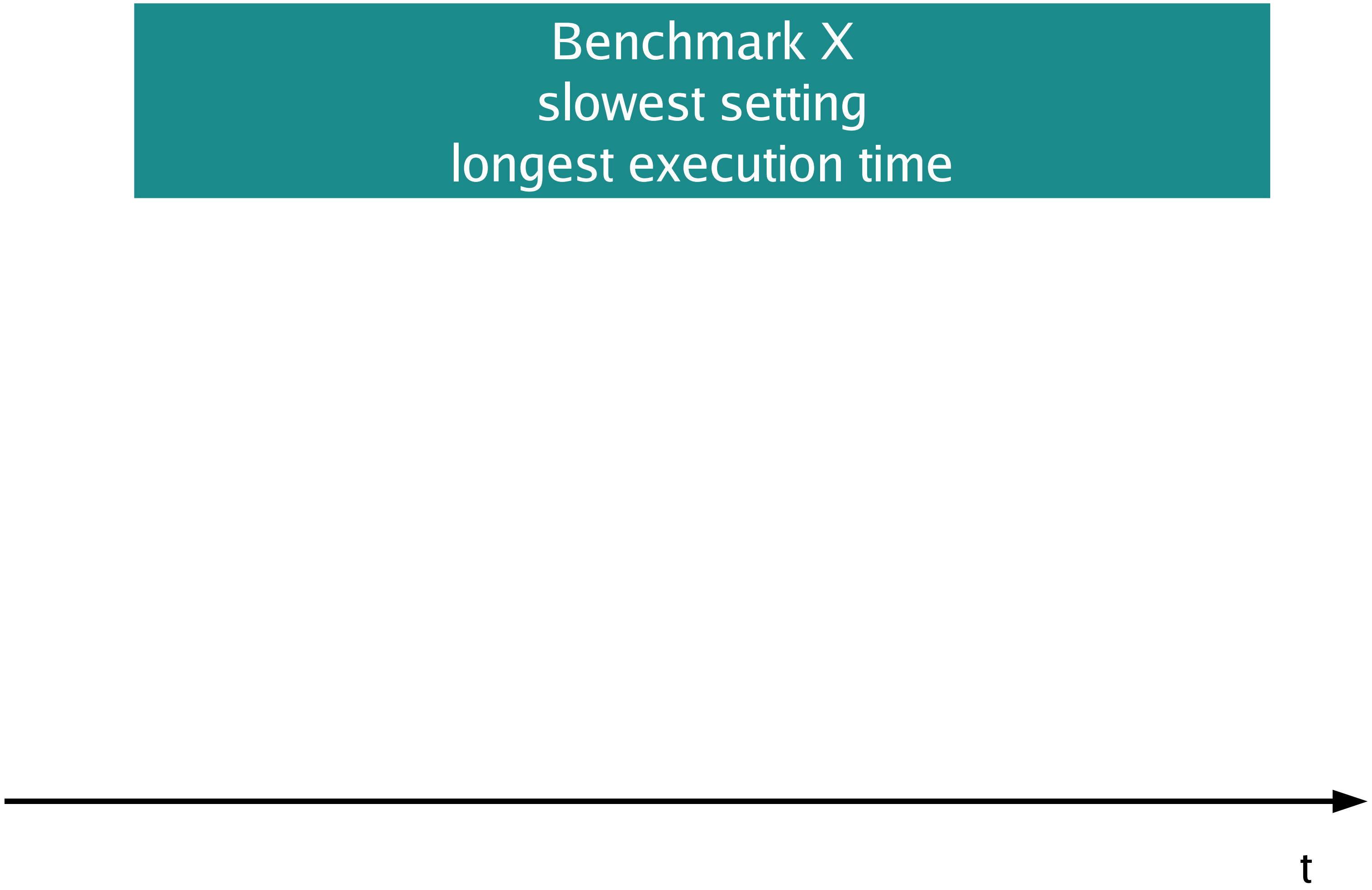
3. NORMALIZED TOTAL ENERGY



3. NORMALIZED TOTAL ENERGY VS NAÏVE MODEL



PADDING WITH IDLE POWER TO EQUAL TOTAL TIME



Benchmark X
slowest setting
longest execution time

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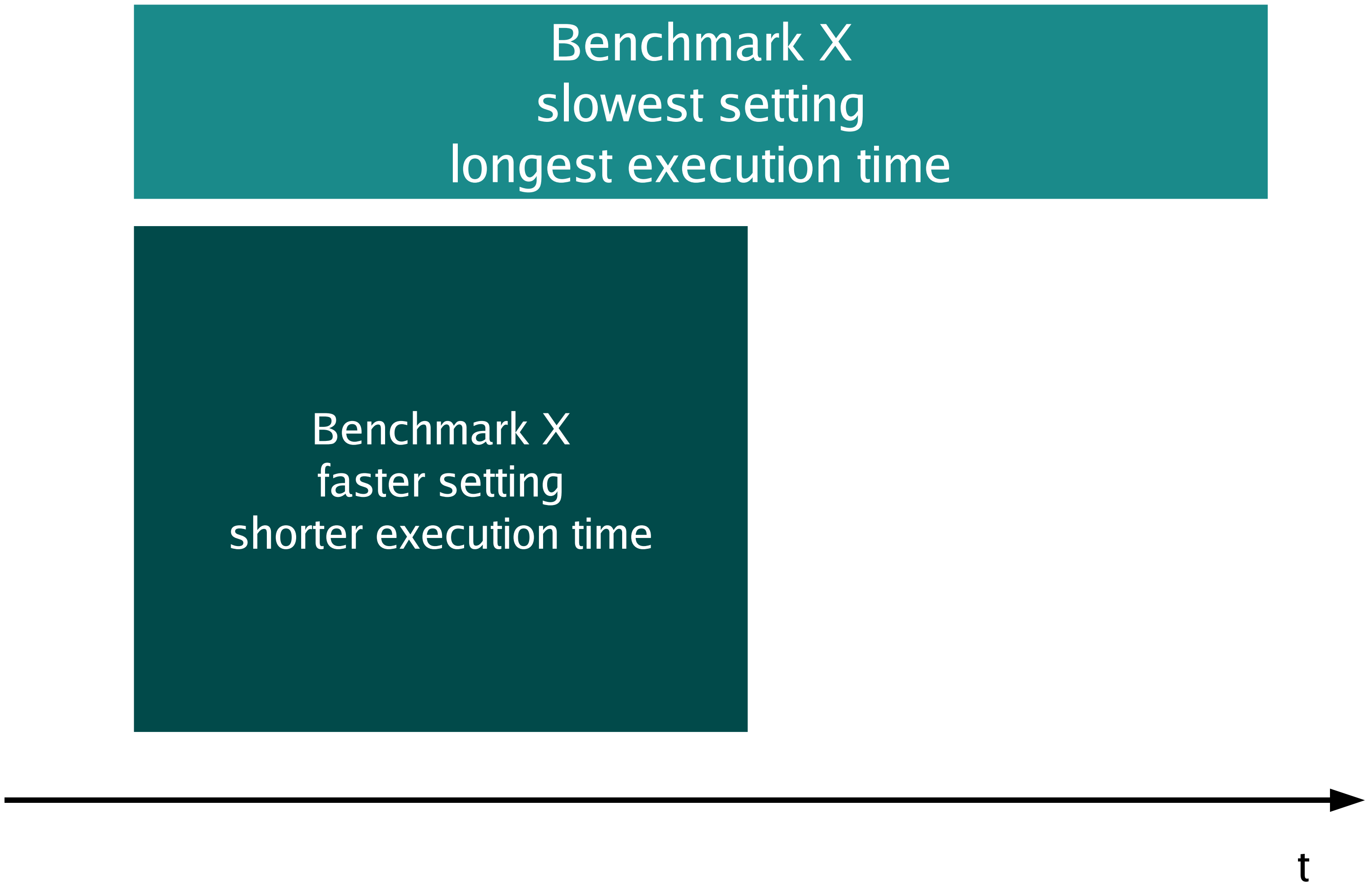

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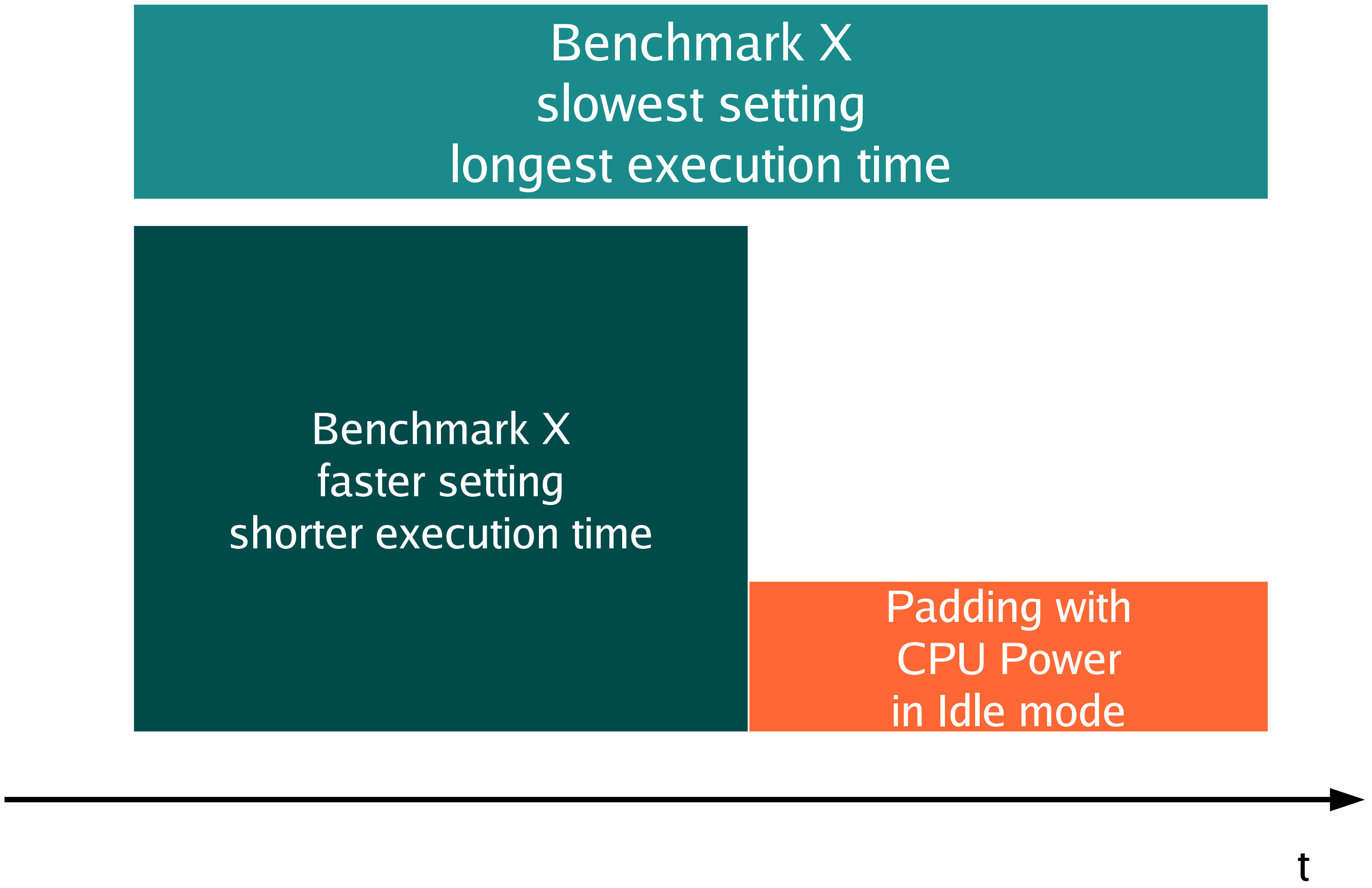

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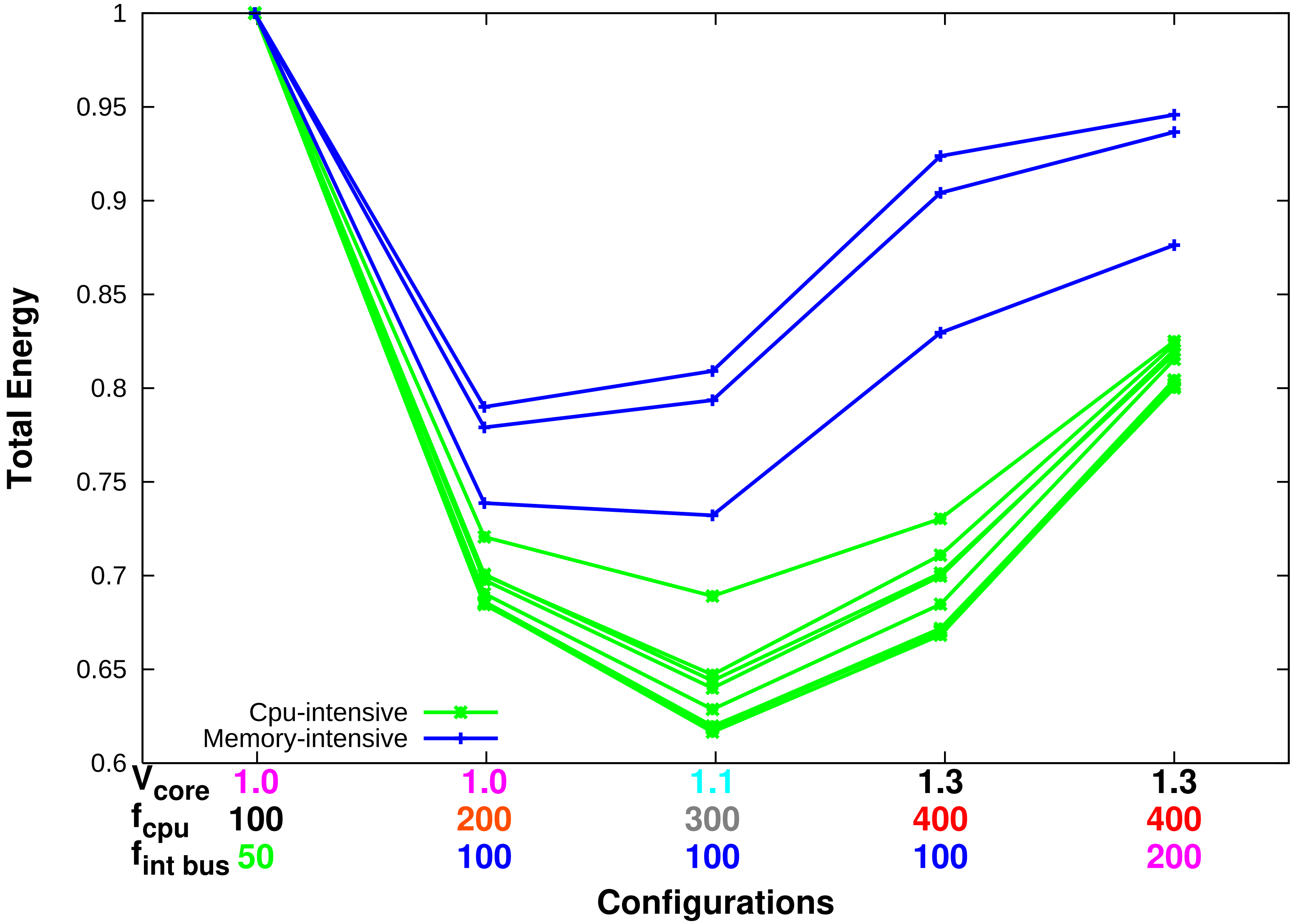
Padding with
CPU Power
in Idle mode

4. NORMALISED TOTAL ENERGY PADDED TO EQUAL TIME



MEMORY POWER ESTIMATION

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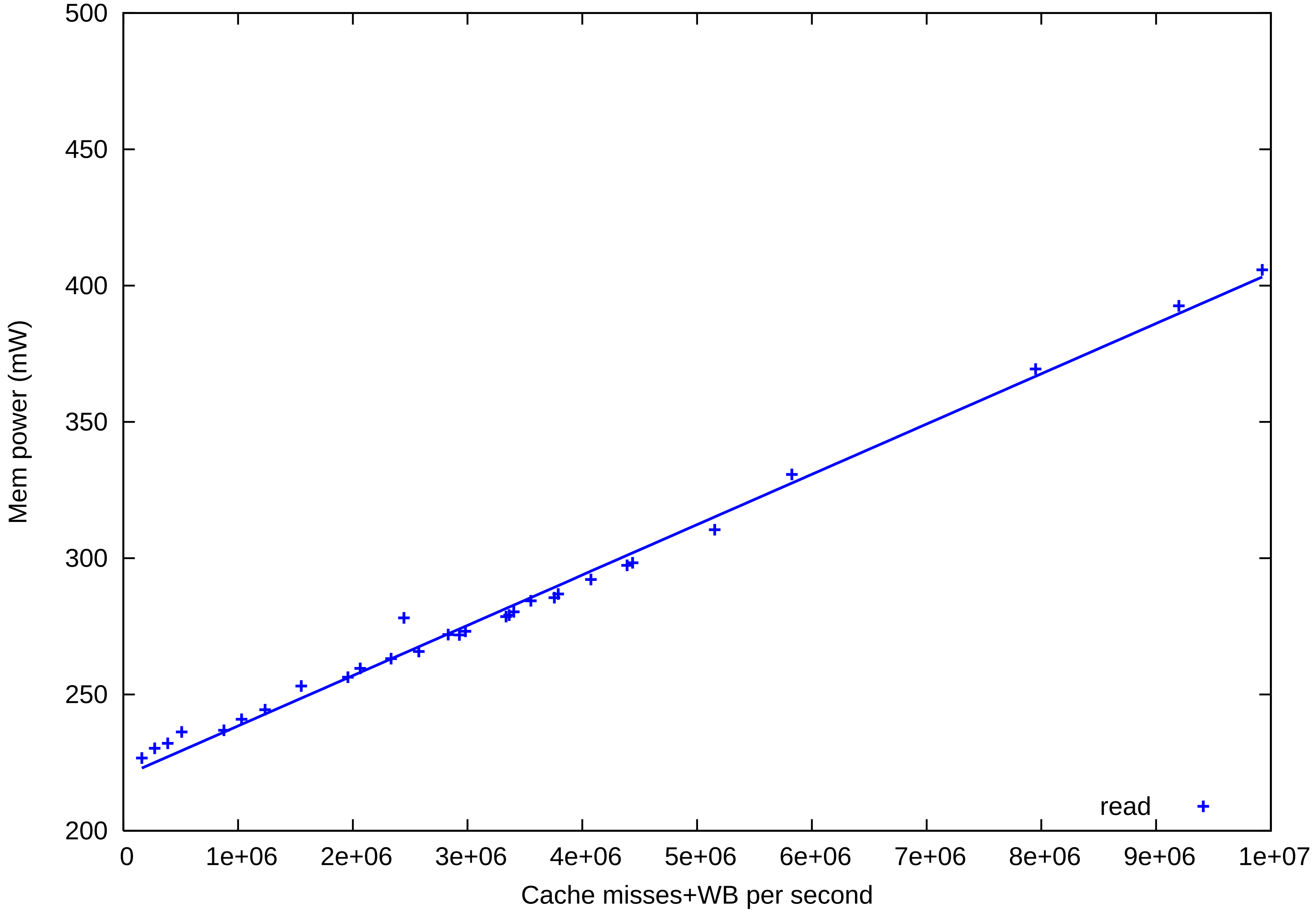
Cache misses can predict memory accesses ?

Investigated via two micro-benchmarks

- *read*: only load instructions
- *modify*: load and then store to same location

5. MEMORY POWER VS CACHE MISS RATE



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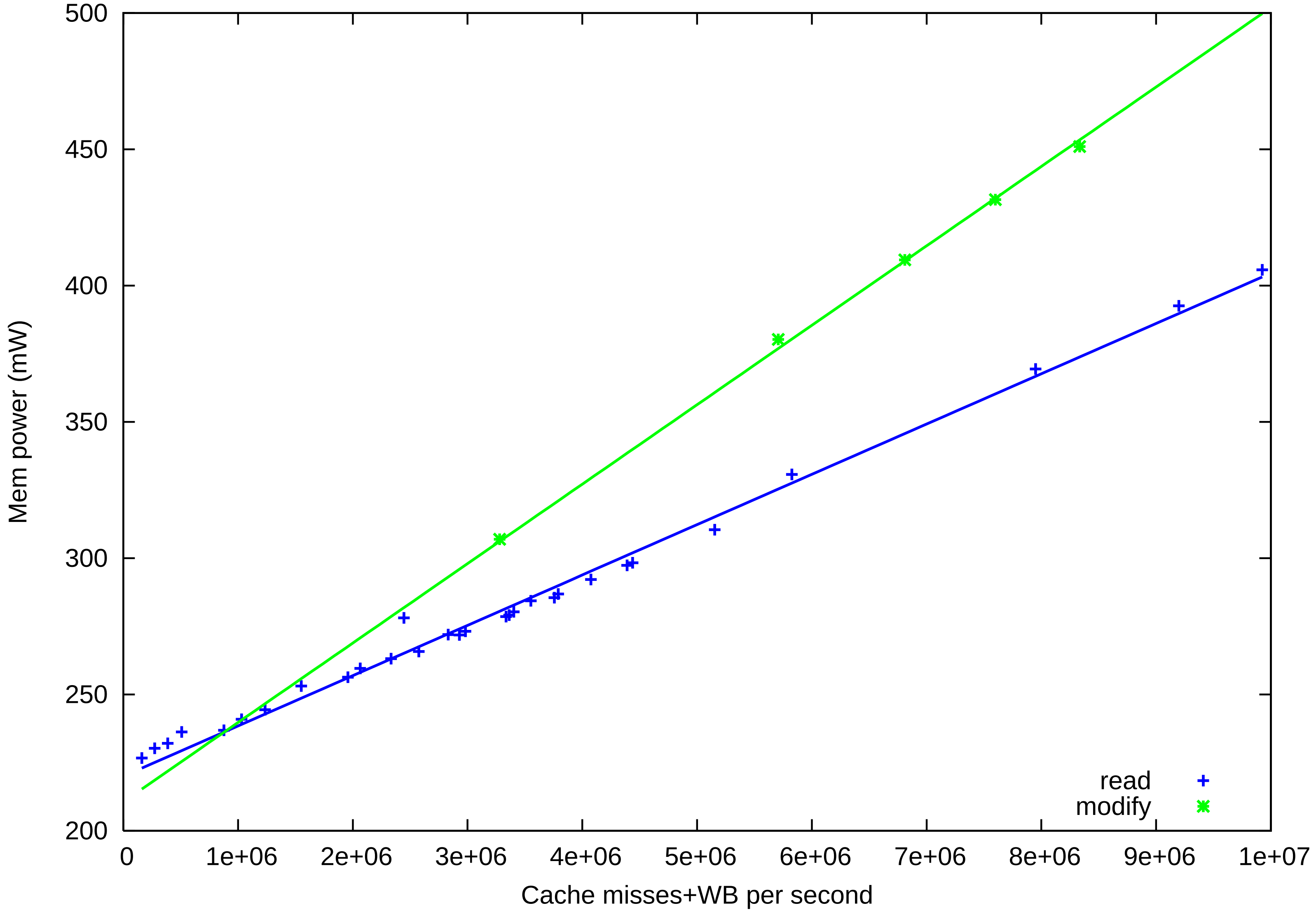

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Future Work

Mechanism and policies for real-time power management